Assignment no 04: Chapter 5

Note: You can check the exercises after the book Chapter. In our assignment, we are using the 11th edition of "Digital Fundamentals" By Thomas L. Floyd"

2. Write the output expression for each circuit in Figure 5–54.

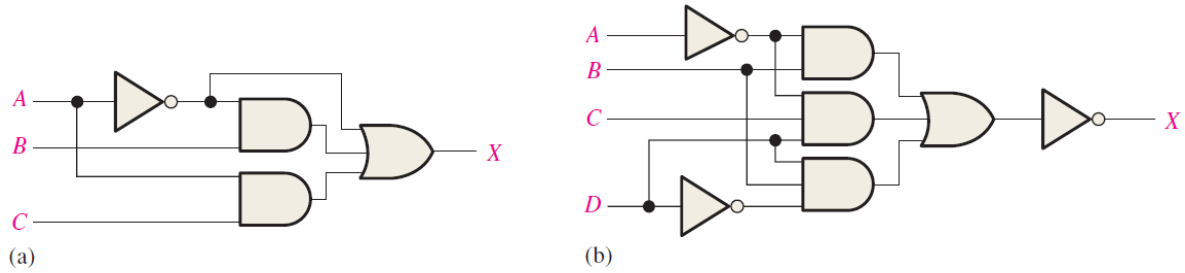

Figure 5–54

4. Write the output expression for each circuit as it appears in Figure 5–56 and then change each circuit to an equivalent AND-OR configuration.

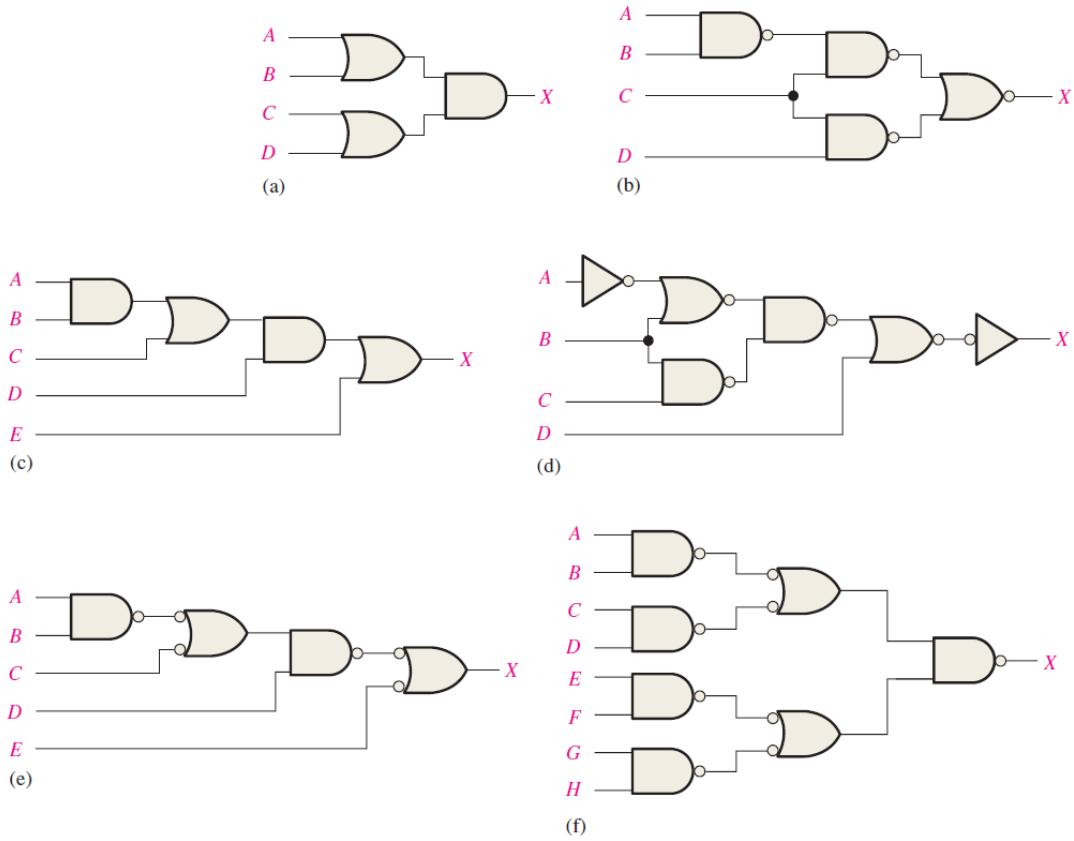

Figure 5–56

6. **Develop** the truth table for each circuit in Figure 5–56.

7. **Show** that an exclusive-NOR circuit produces a POS output.

10. Use AND gates, OR gates, or combinations of both to **implement** the following logic expressions as stated:

(a) $X = A + B + C$
(b) $X = ABC$
(c) $X = A + BC$
(d) $X = AB + CD$
(e) $X = (A + B)(C + D)$
(f) $X = A + BCD$
(g) $X = ABC + BCD + DEF$
(h) $X = ABC(D + E + F) + AC(C + D + E)$

12. Use NAND gates, NOR gates, or combinations of both to **implement** the following logic expressions as stated:

(a) $X = \overline{A}B + CD + \overline{(A + B)}(ACD + \overline{BE})$
(b) $X = AB\overline{C}\,\overline{D} + D\overline{E}F + \overline{A}F$
(c) $X = \overline{A}[B + \overline{C}(D + E)]$

14. **Implement** a logic circuit for the truth table in Table 5–9.

TABLE 5–9

Inputs				Output
A	*B*	*C*	*D*	*X*
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

20. **Implement** the logic circuits in Figure 5–54 using only NAND gates.

22. **Repeat** Problem 20 using only NOR gates.

24. **Show** how the following expressions can be implemented as stated using only NOR gates:

(a) $X = ABC$ **(b)** $X = \overline{ABC}$ **(c)** $X = A + B$
(d) $X = A + B + \overline{C}$ **(e)** $X = \overline{AB} + \overline{CD}$ **(f)** $X = (A + B)(C + D)$
(g) $X = AB[C(\overline{DE} + \overline{AB}) + \overline{BCE}]$

26. **Implement** each function in Problem 10 by using only NAND gates.

30. For the input waveforms in Figure 5–61, **what** logic circuit will generate the output waveform shown?

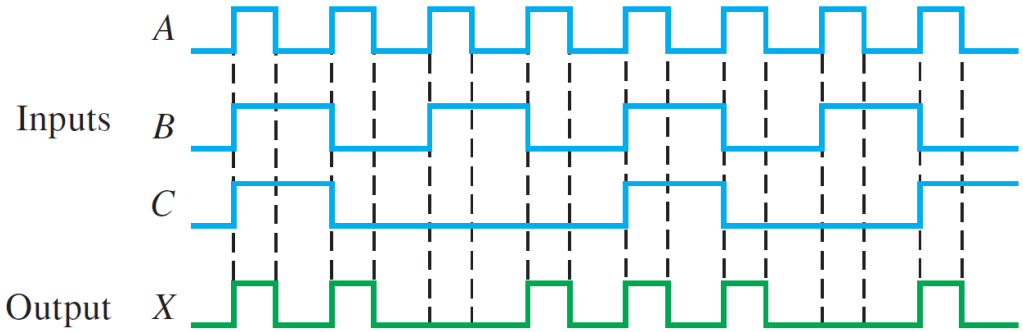

Figure 5–61